

## Challenges for nanomaterials in the semiconductor industry of the post-nanometer era

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The naming conventions employed by leading semiconductor foundries to describe the next generation of nanoelectronics signal the dawn of the Angstrom era. The unit ( $\text{\AA}$ ) is used to measure atoms, and ionic radius with  $1\text{\AA}$  roughly equal to the diameter of one atom, or 0.1 nm. Although discrete manufacturing at this scale is still unattainable, the design of the upcoming logic and memory devices revolves around increasingly smaller architectures, incorporating three-dimensional structures and a wider range of materials.

Anticipated advancements in transistor design include the transition from FinFET, projected to persist until the 3nm node, to Gate-all-around (GAA) and nanosheets designs at 2nm, followed by groundbreaking concepts like vertical, stackable architectures, and atomic channels at 1nm and beyond. Consequently, evaluating the properties of materials at the nanometer scale to establish correlations with device functionality, reliability, and failures presents a significant challenge for the scientific community. This highlights the imperative to develop innovative techniques and methodologies that leverage the principles of physics, enabling us to tackle engineering problems that were once deemed insurmountable.

In this context, I will provide an overview of potential future scenarios for the roadmap, offering a comprehensive perspective on critical issues regarding materials integration and metrology. We will explore various areas of research in the semiconductor industry that aim to merge our current capabilities in materials characterization with correlative, site-specific metrology, and failure analysis techniques for state-of-the-art logic and memory chips.